ABSTRACT OF THE DISCLOSURE

In a data processor, a pickup head reads the data from a memory medium. Such data transferred in a plurality of parallel bits in synchronization with the clock signal to a controller unit from a read channel unit. The controller unit detects the predetermined mark for detecting synchronization included in the data in order to establish the synchronization of a series of data to be received from the read channel unit in order to demodulate the data other than the predetermined mark for detecting synchronization. The mark detecting unit in the controller unit detects the predetermined mark for detecting synchronization from the parallel data received with the shift register.